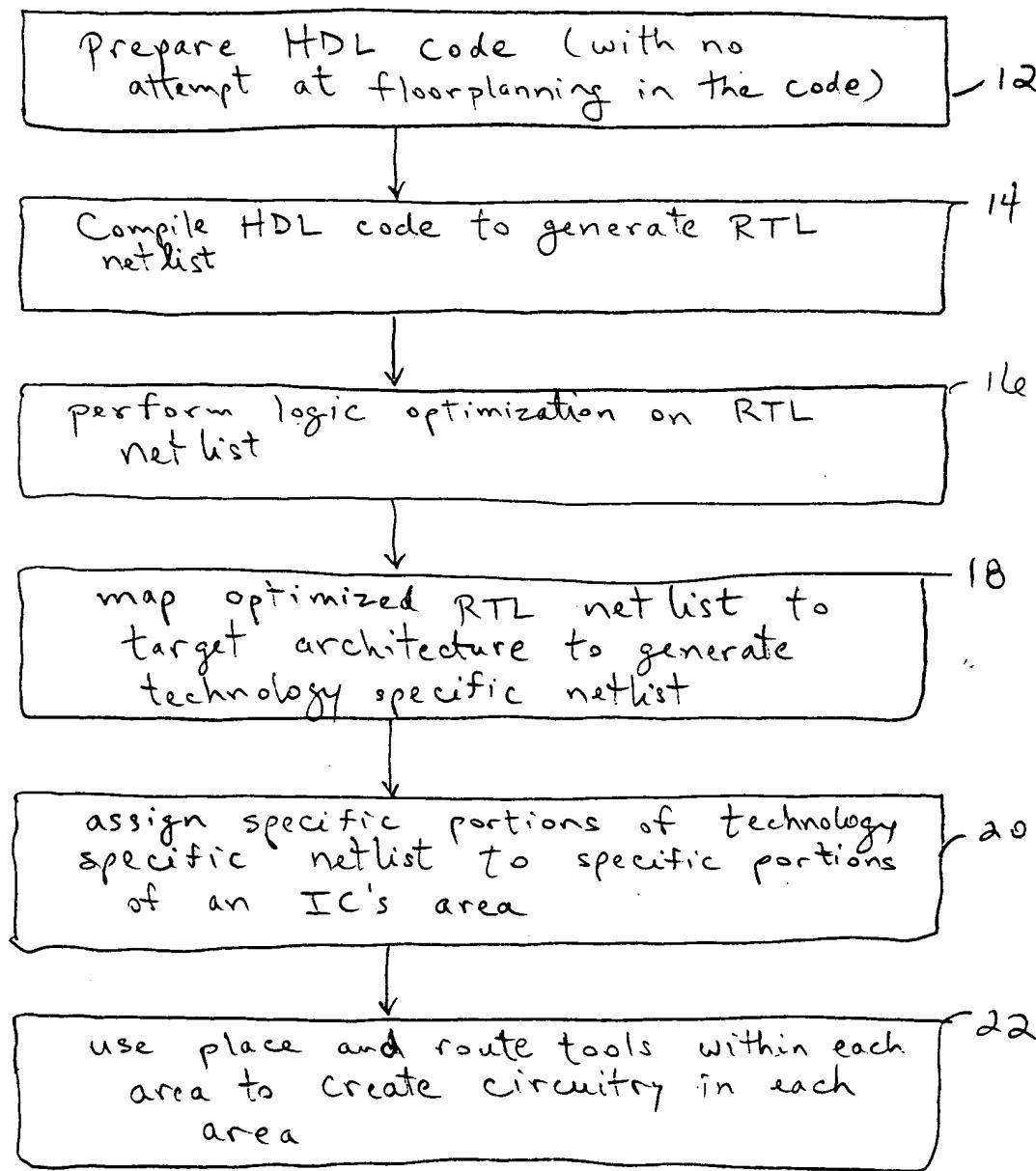


FIG. 1A (Prior Art)

10



12

14

16

18

20

22

30figs

Fig. 1B (Prior Art)

25

Prepare HDL code for first preselected region of an IC

26

Prepare HDL code for second preselected region of the IC

28

Prepare interconnect HDL code for interconnects between two regions of the IC

30

Perform separately synthesis for each region

32

(for each region, compile HDL code, optimize logic and map to target architecture)

and perform synthesis of interconnect HDL code

34

Use place and route tools within each region to create circuitry in each region

13-782 500 SHEETS, FILLER, 5 SQUARE
42-381 100 SHEETS, EYE, EASE, 5 SQUARE
42-382 200 SHEETS, EYE, EASE, 5 SQUARE
42-389 100 RECYCLED, WHITE, 5 SQUARE
42-392 200 RECYCLED, WHITE, 5 SQUARE
PRINTED IN U.S.A.

National Brand

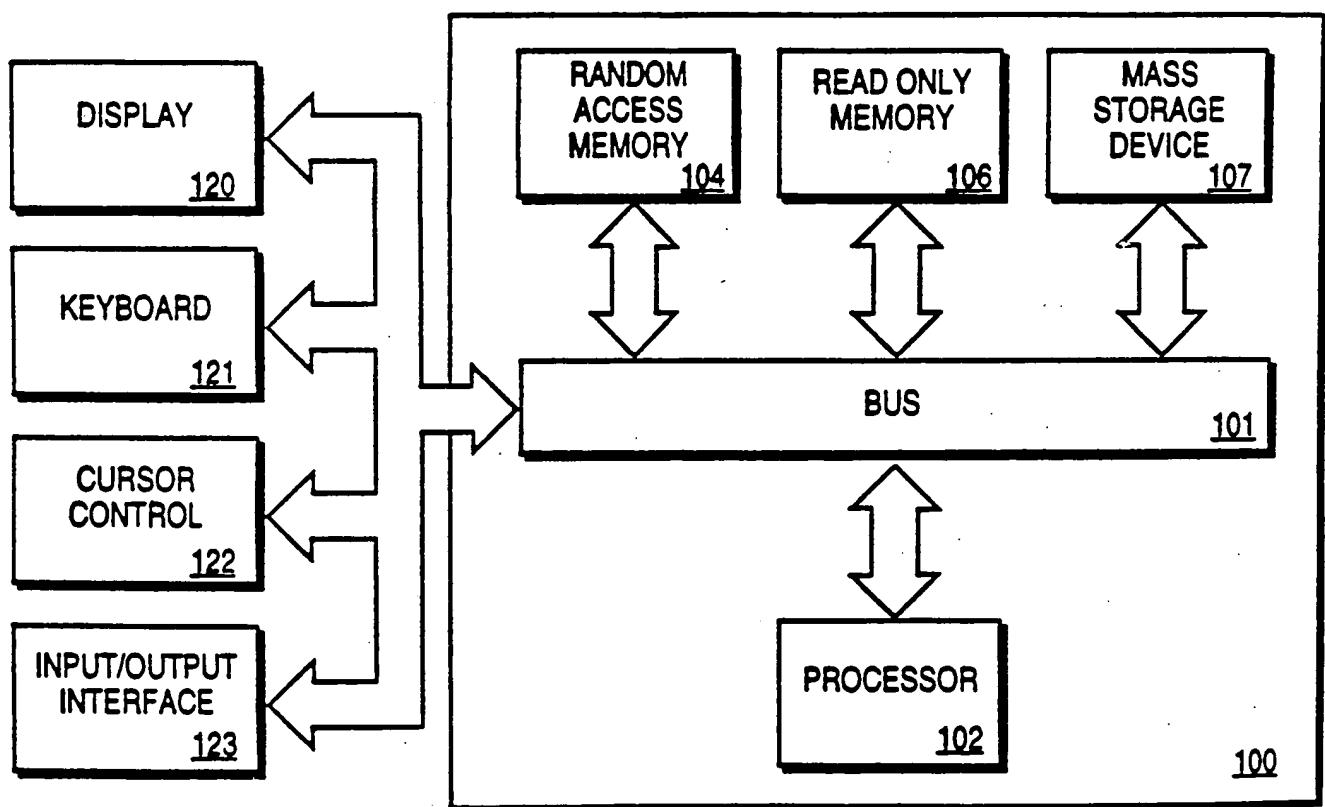


FIG. 2

Fig. 3

201

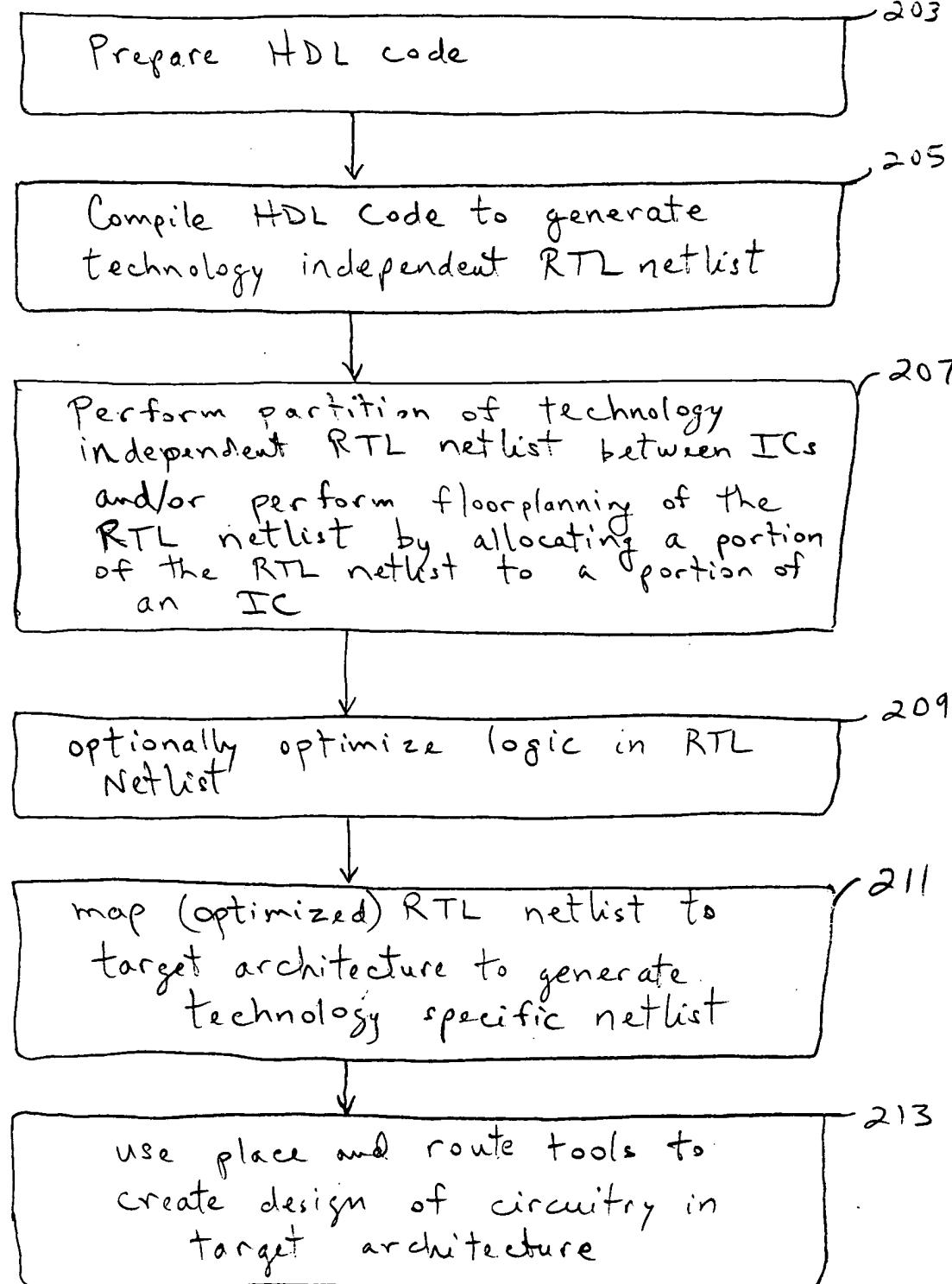


Fig. 4A.

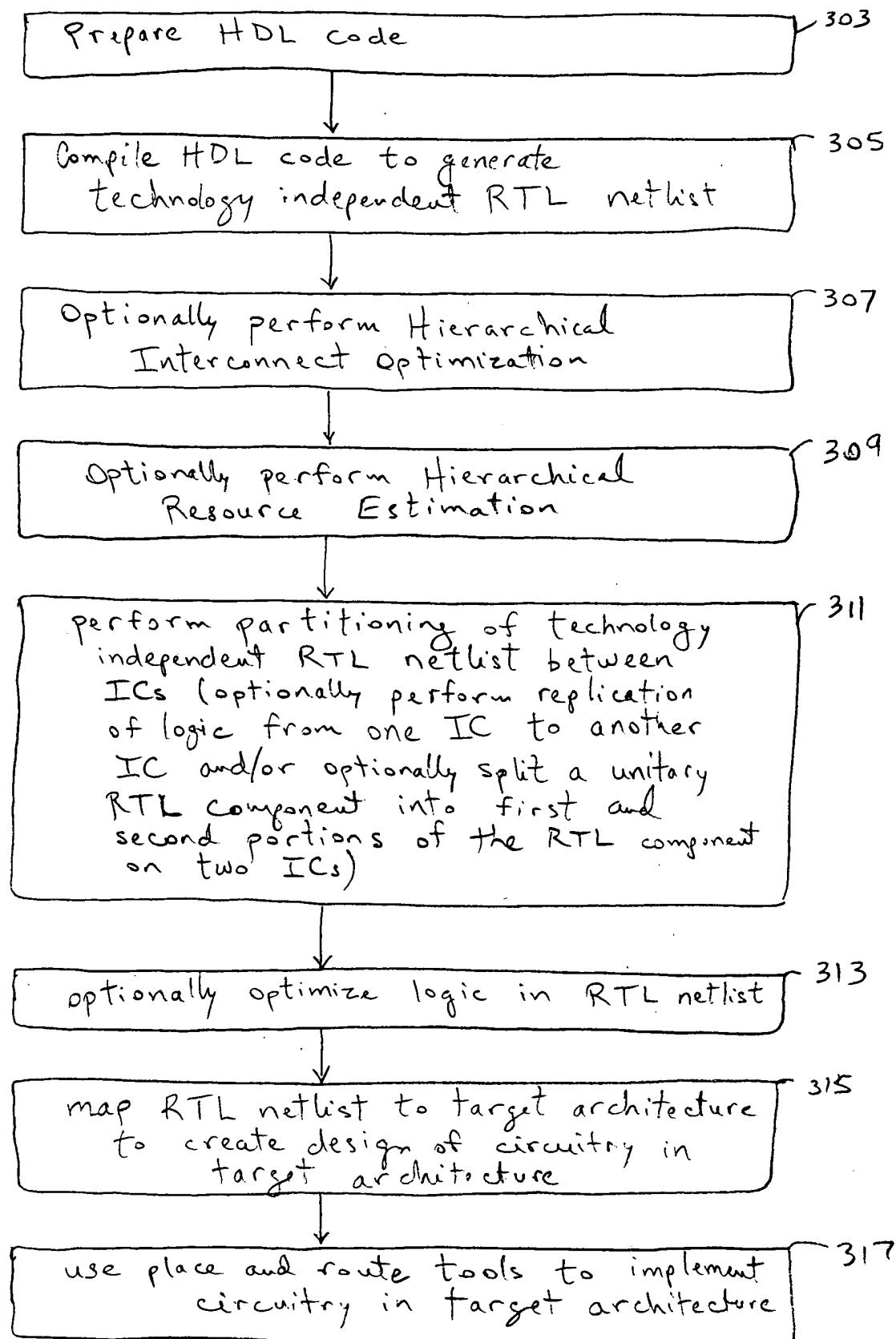
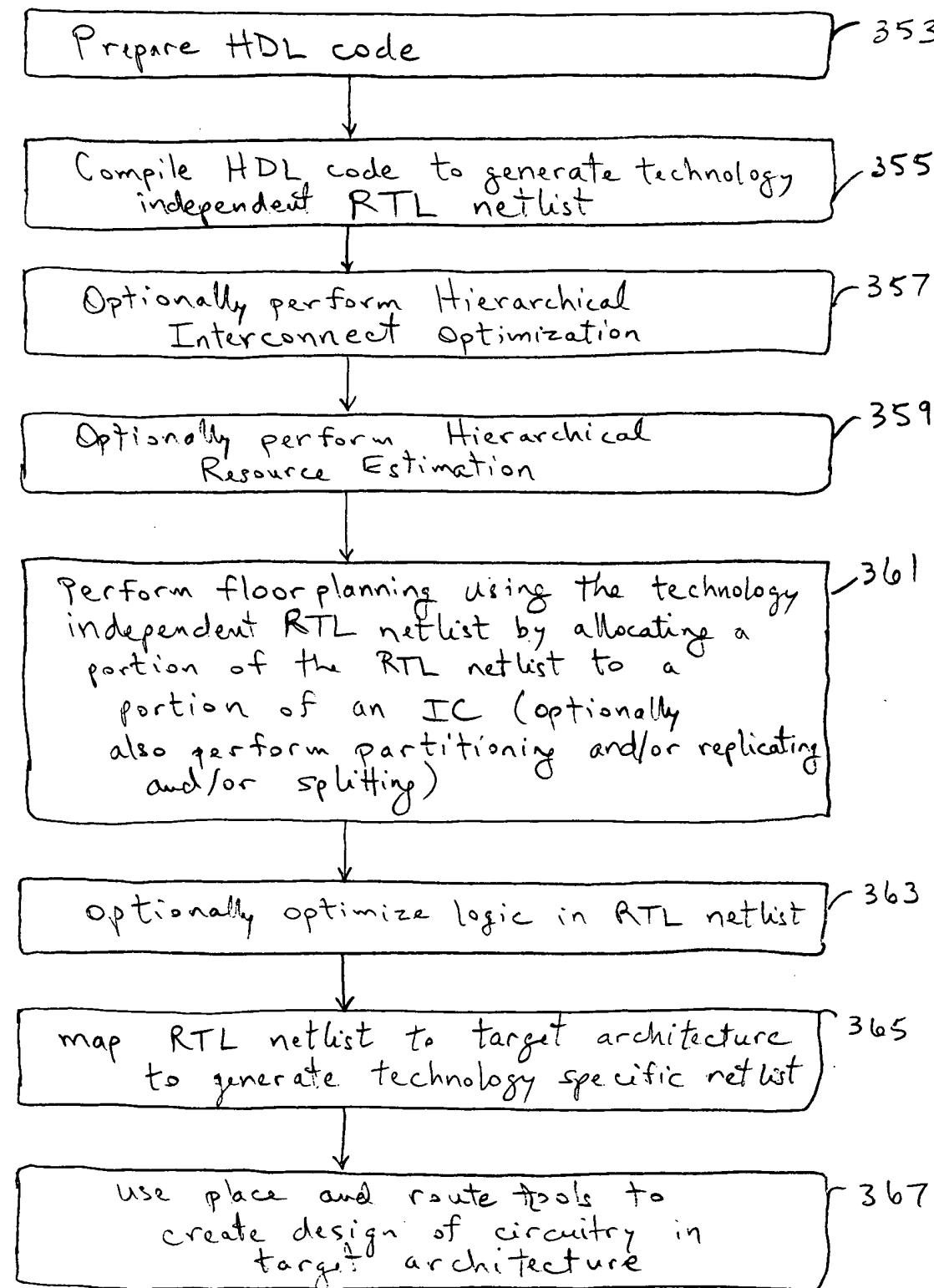


Fig. 4B

351



13.762 500 PEEERS, FILLED 500 SQUARE
12.391 500 PEEERS, FILLED 500 SQUARE
10.532 100 PEEERS, FILLED 100 SQUARE
42.369 200 PEEERS, FILLED 200 SQUARE
42.369 100 RECYCLED WHITE 500 SQUARE
42.369 200 RECYCLED WHITE 500 SQUARE

National Brand
Made in S.A

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FIG. 5A

Hierarchical Interconnect Optimization ⁴⁰¹

Examine Interconnects between RTL
modules resulting from HDL
compilation

⁴⁰³

↓
perform Interconnect optimization
(e.g. remove duplicative I/O's between
modules) at technology
independent RTL netlist level

⁴⁰⁵

Fig. 5.B

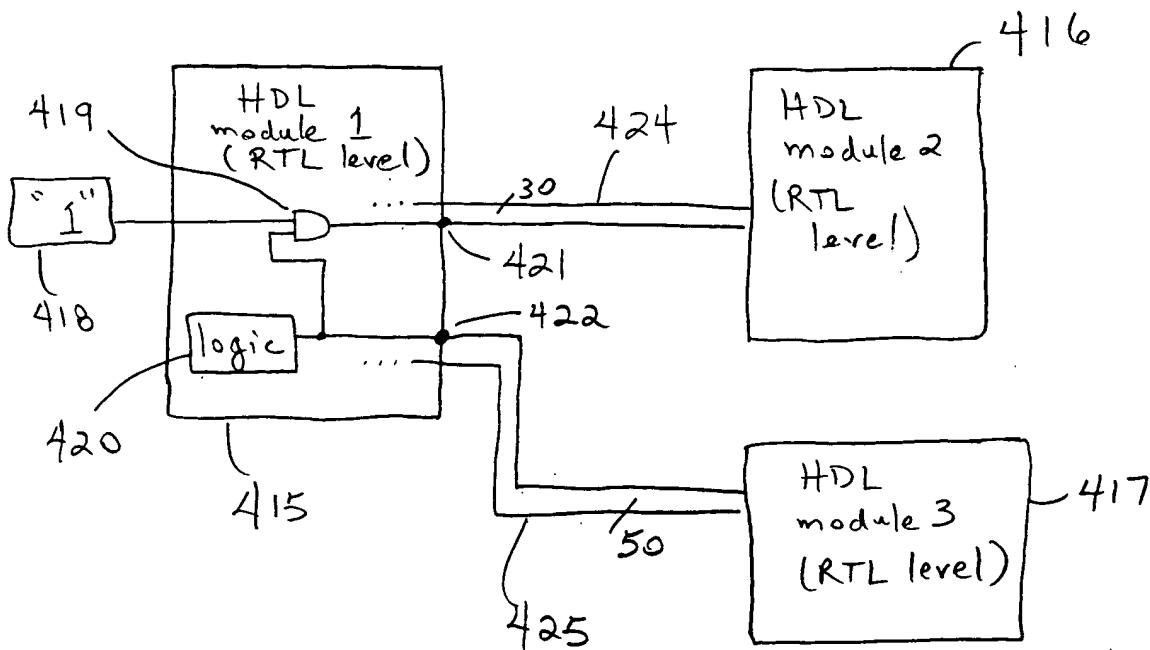


Fig. 6

501

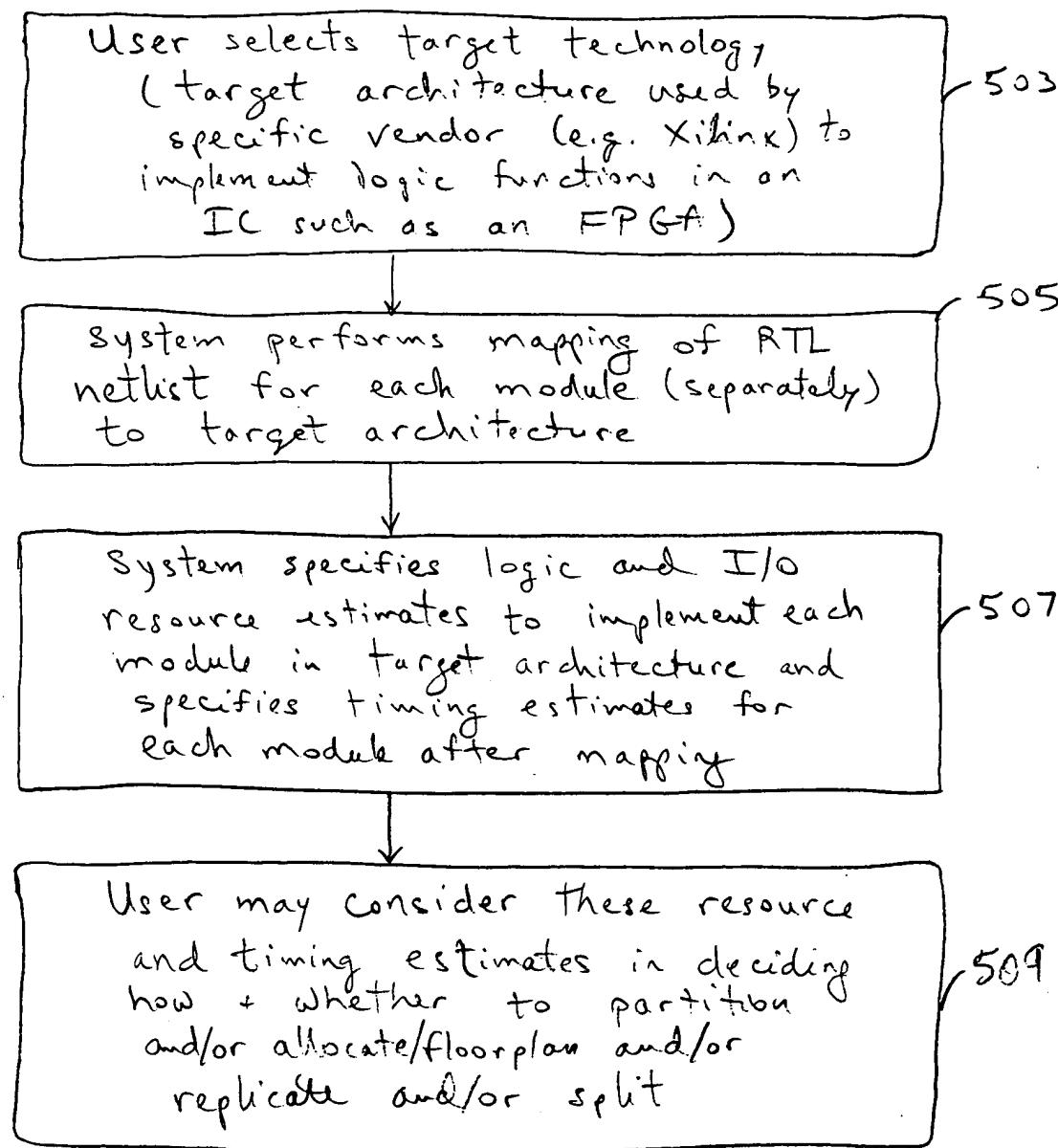


Fig. 7 A

← 601

User (or system automatically) directs a partitioning (and/or floorplanning and/or replicating and/or splitting) by selecting/assigning an RTL netlist module to another IC (e.g. a 2nd IC)

→ 603

System replicates signals between/among ICs (e.g. common input signals)

→ 605

System creates new RTL netlist for each IC (e.g. new I/O pins, logic etc.)

→ 607

13762 500 SQUARE, FULL 5 SQUARE
42392 500 SQUARE, FULL 5 SQUARE
42392 100 SQUARE, FULL 5 SQUARE
42392 200 SQUARE, FULL 5 SQUARE
42399 100 RECYCLED WHITE 5 SQUARE
42399 200 RECYCLED WHITE 5 SQUARE

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Fig. 7B

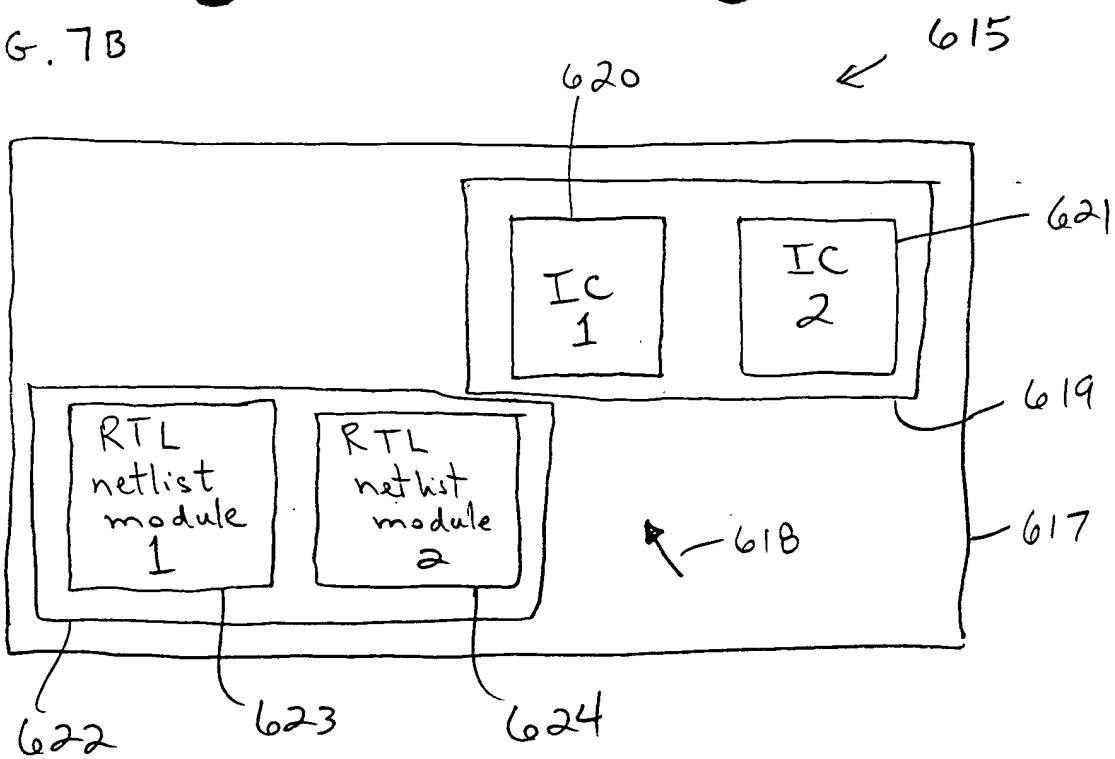


Fig. 8A

701

```

module prep2_2 (DATA0, DATA1, DATA2, LDPRE, SEL, RST, CLK, LDCOMP);
output [7:0] DATA0 ;
input [7:0] DATA1, DATA2;
input LDPRE, SEL, RST, CLK, LDCOMP;
wire [7:0] DATA0_internal;
prep2_1 inst1 (CLK, RST, SEL, LDCOMP, LDPRE, DATA1, DATA2, DATA0_internal);
prep2_1 inst2 (CLK, RST, SEL, LDCOMP, LDPRE, DATA0_internal, DATA2, DATA0);
endmodule

```

- 703

```

module prep2_1 (CLK, RST, SEL, LDCOMP, LDPRE, DATA1, DATA2, DATA0);
input CLK, RST, SEL, LDCOMP, LDPRE ;
input [7:0] DATA1, DATA2 ;
output [7:0] DATA0;
reg [7:0] DATA0;
reg [7:0] highreg_output, lowreg_output; // internal registers
wire compare_output = (DATA0 == lowreg_output); // comparator
wire [7:0] mux_output = SEL ? DATA1 : highreg_output; // mux
// registers
always @ (posedge CLK or posedge RST)
begin
  if (RST) begin
    highreg_output = 0;
    lowreg_output = 0;
  end else begin
    if (LDPRE)
      highreg_output = DATA2;
    if (LDCOMP)
      lowreg_output = DATA2;
  end
end
// counter
always @ (posedge CLK or posedge RST)
begin
  if (RST)
    DATA0 = 0;
  else if (compare_output) // load
    DATA0 = mux_output;
  else
    DATA0 = DATA0 + 1;
end
endmodule

```

- 705

FIG. 8B

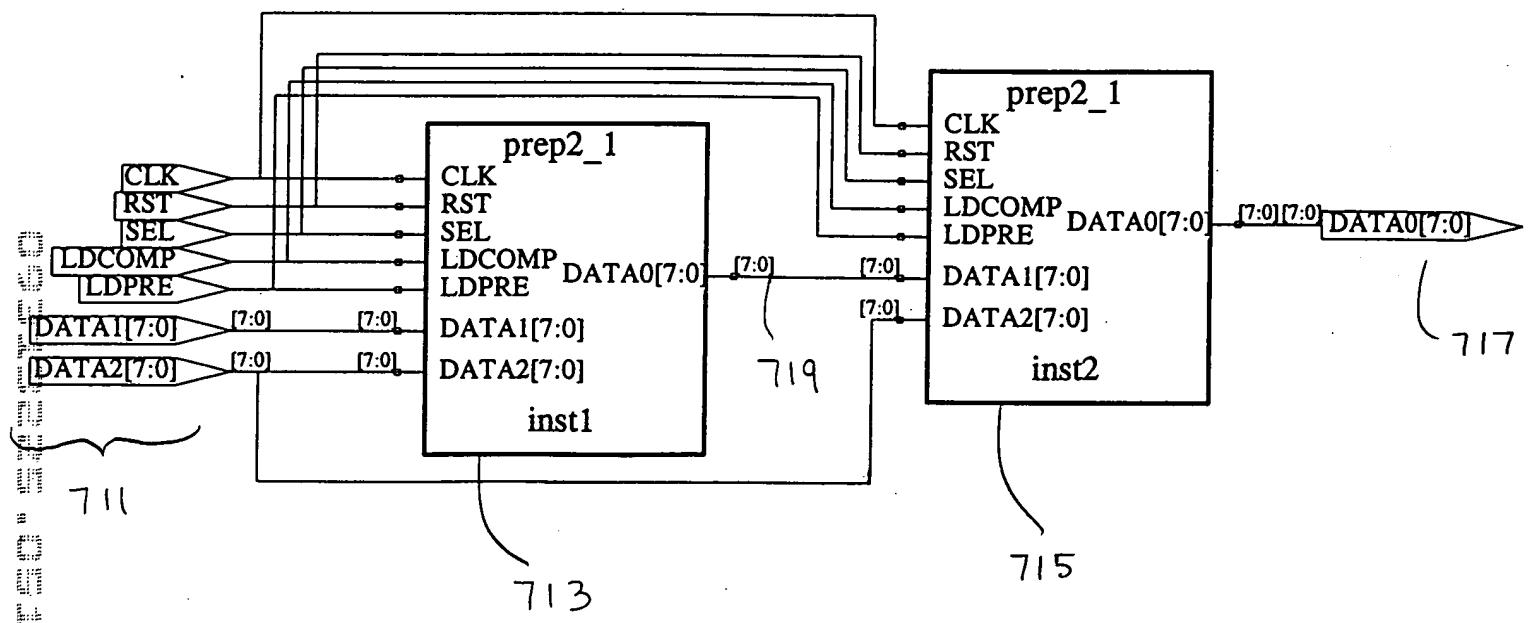


FIG. 8 C

713

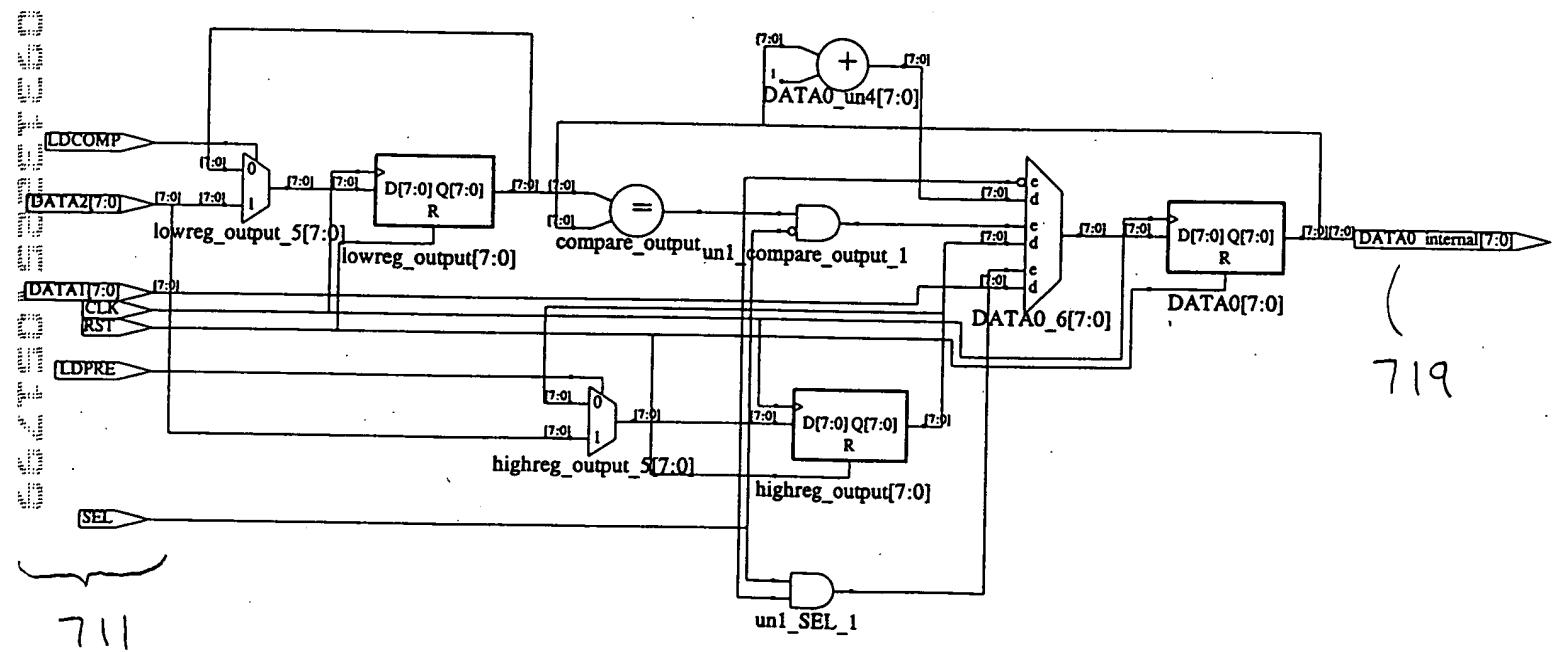


FIG. 8D

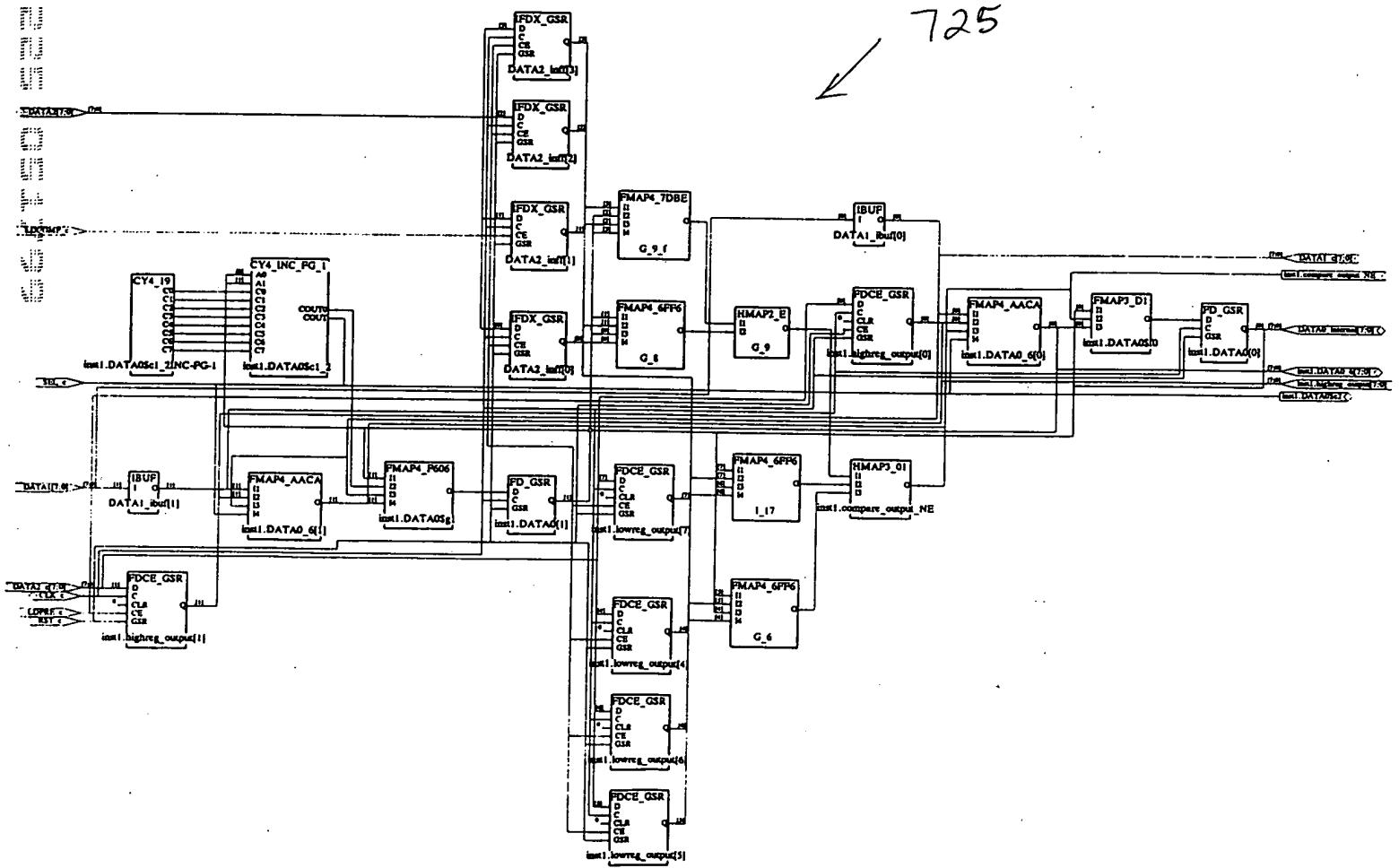


FIG. 9 A

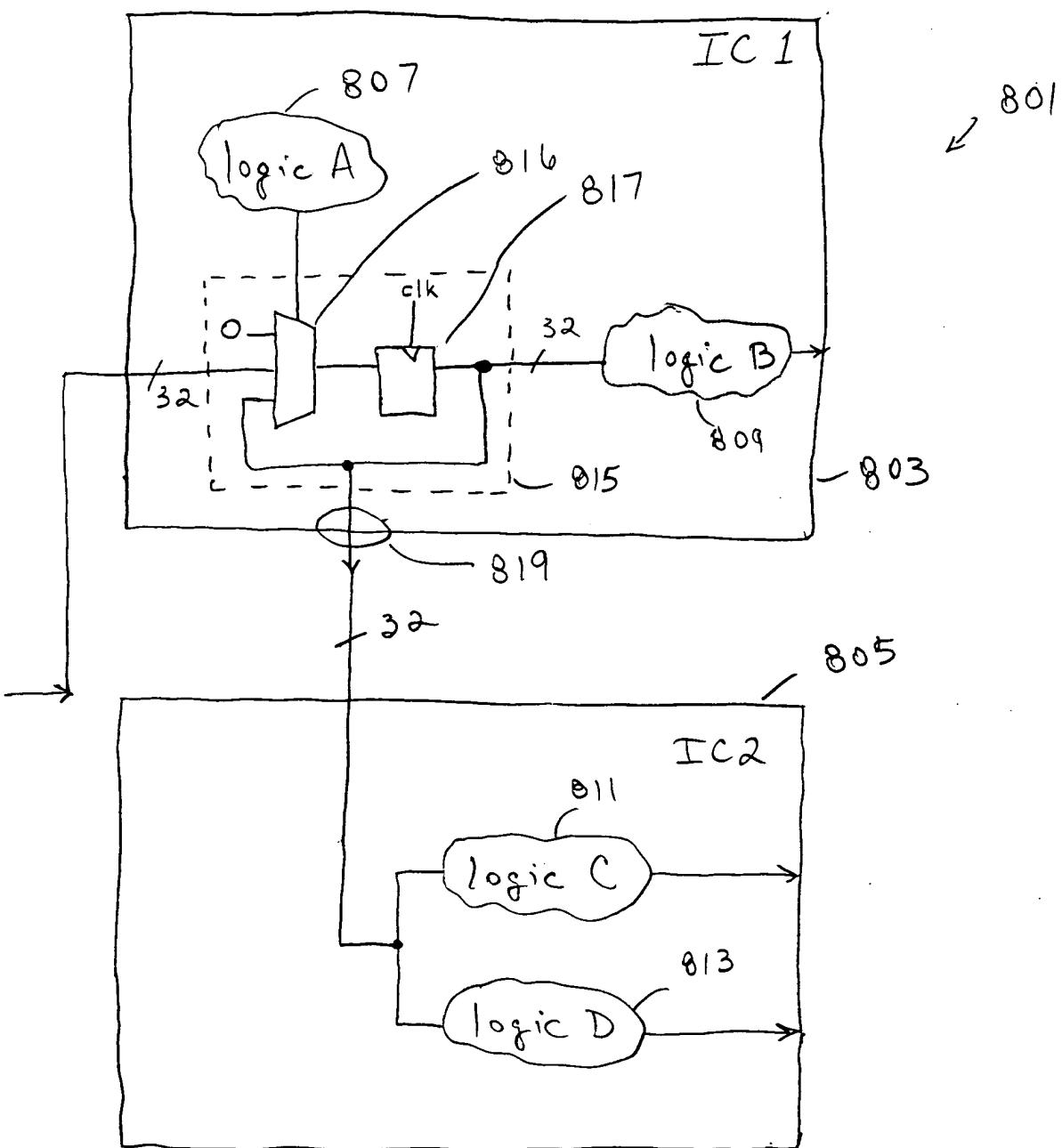


FIG. 9B

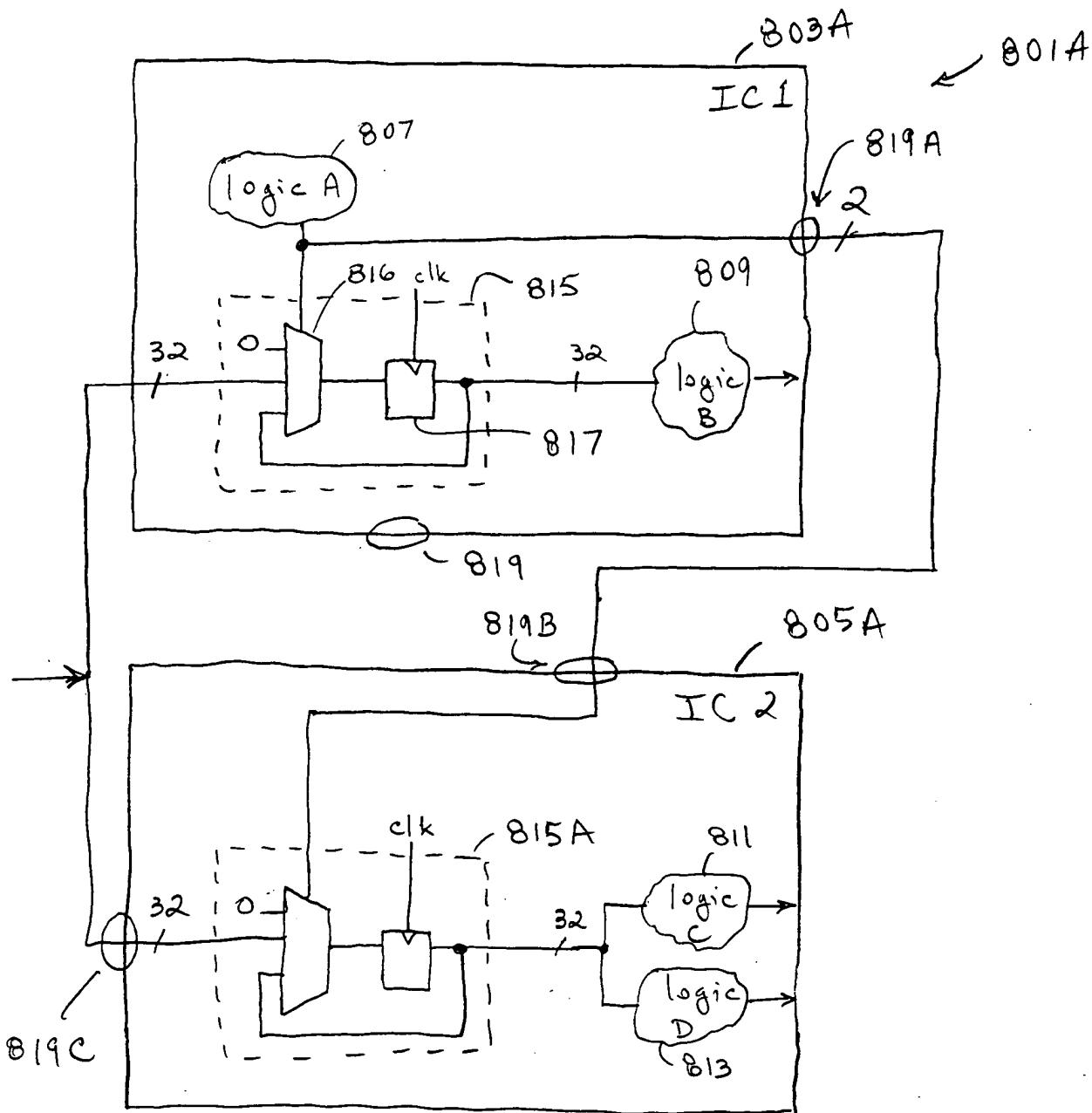


FIG. 9 C

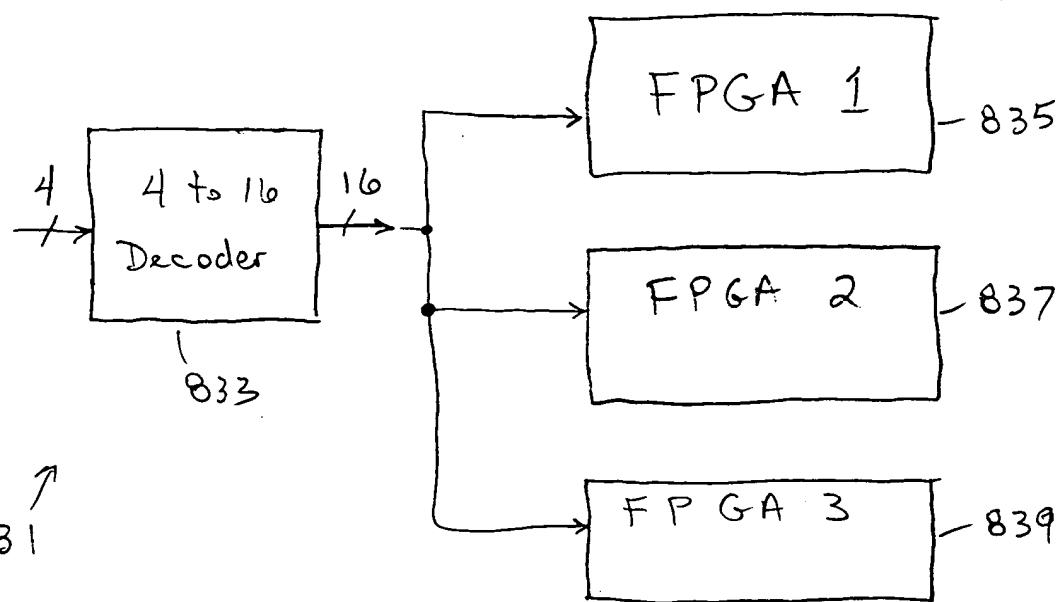


FIG. 9 D

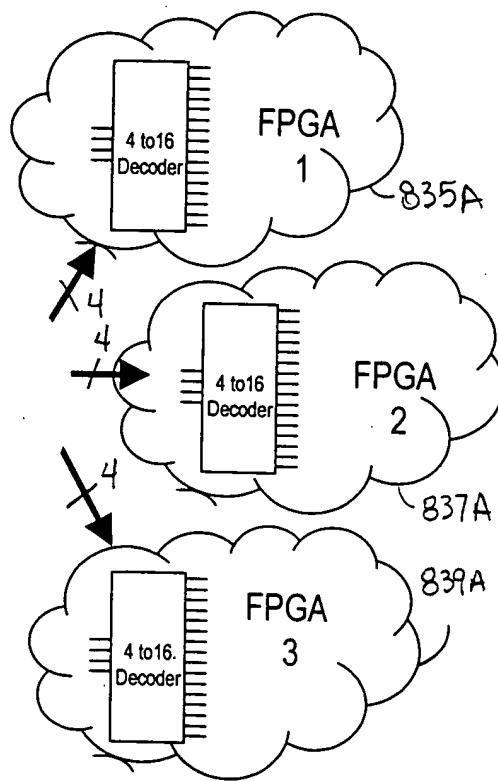


FIG. 9 E

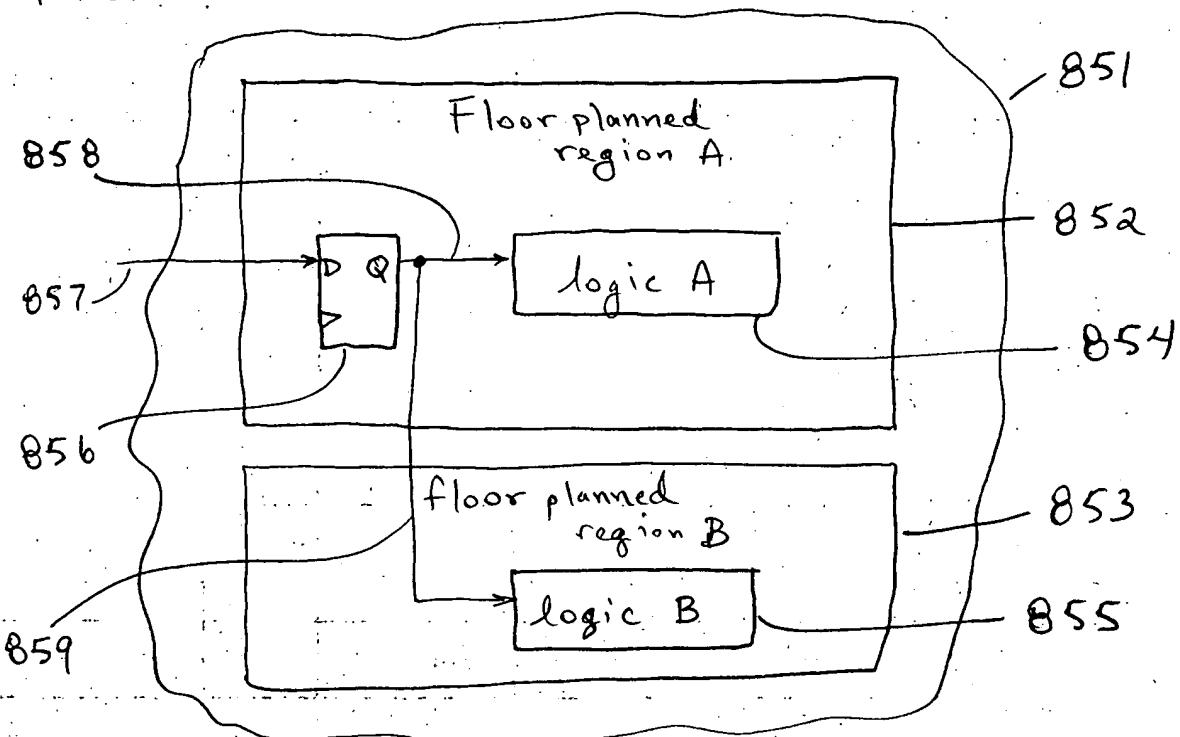


Fig. 9 F

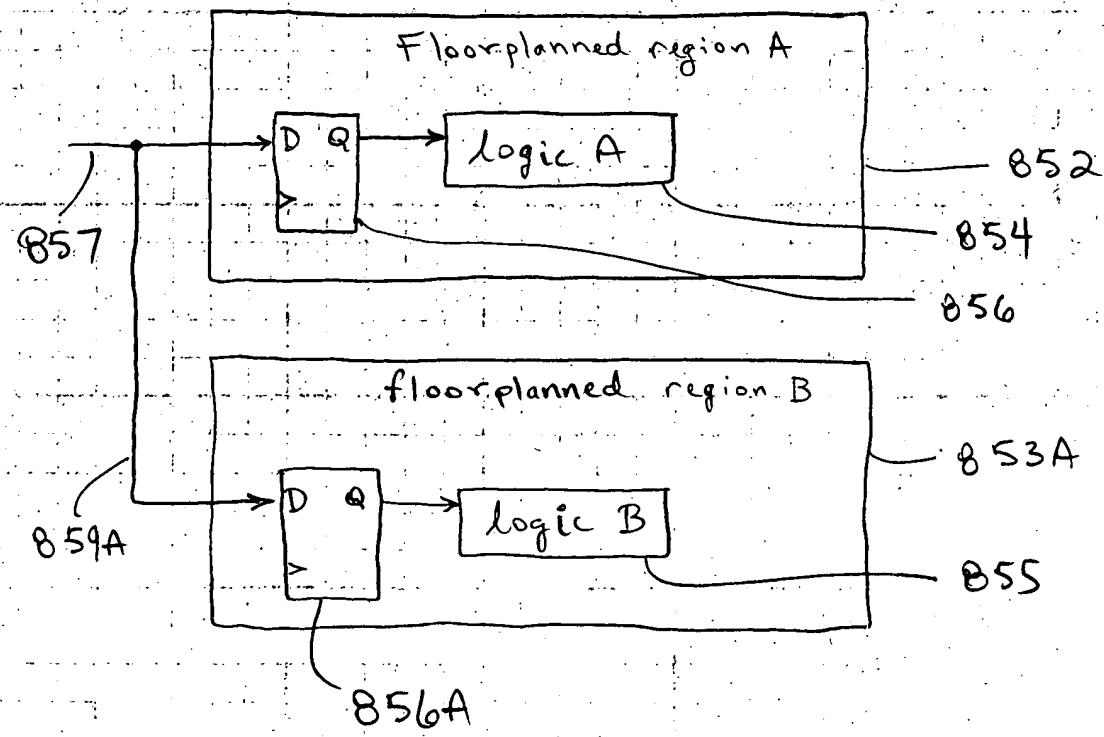


Fig. 10 A

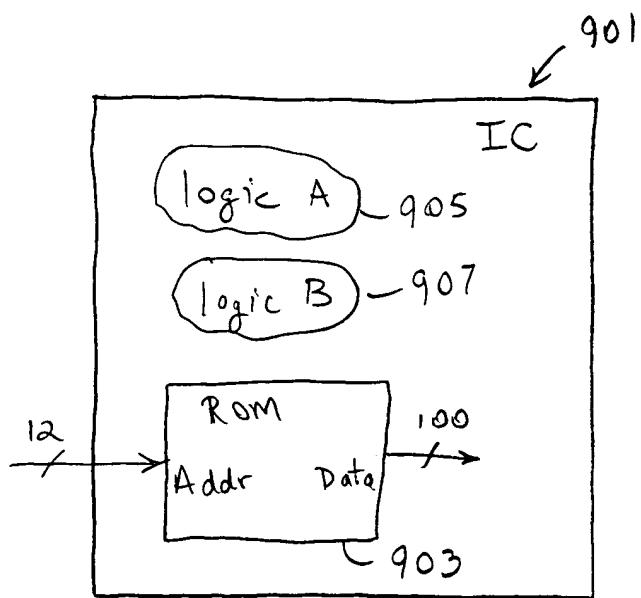


Fig. 10 B

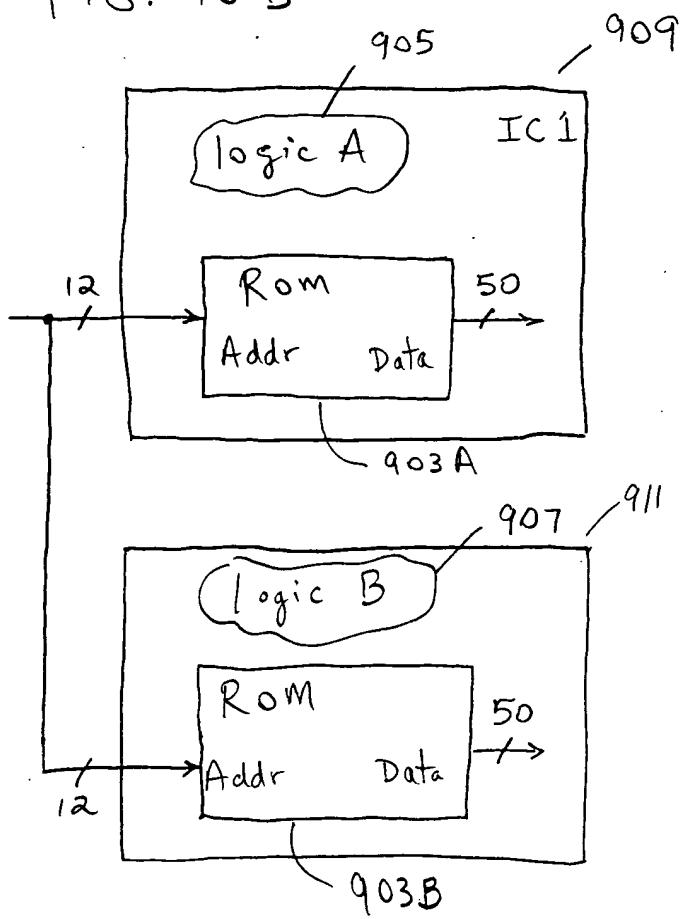


FIG. 10 C

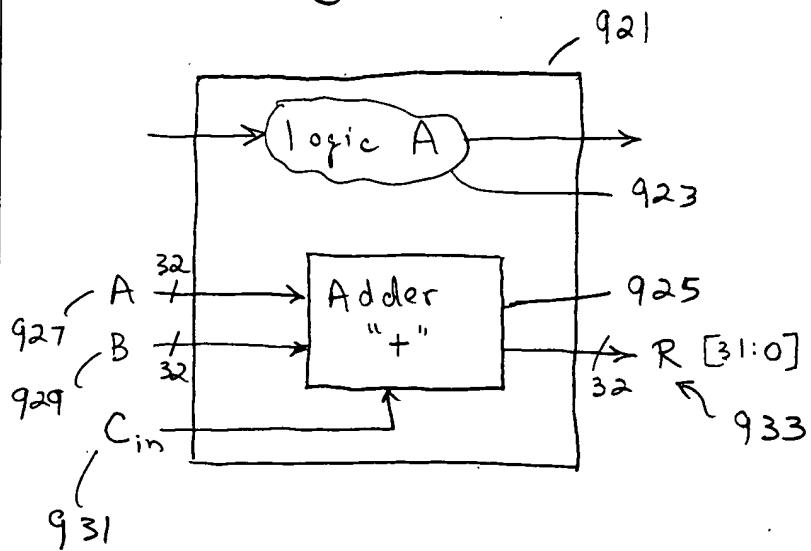


FIG. 10 D

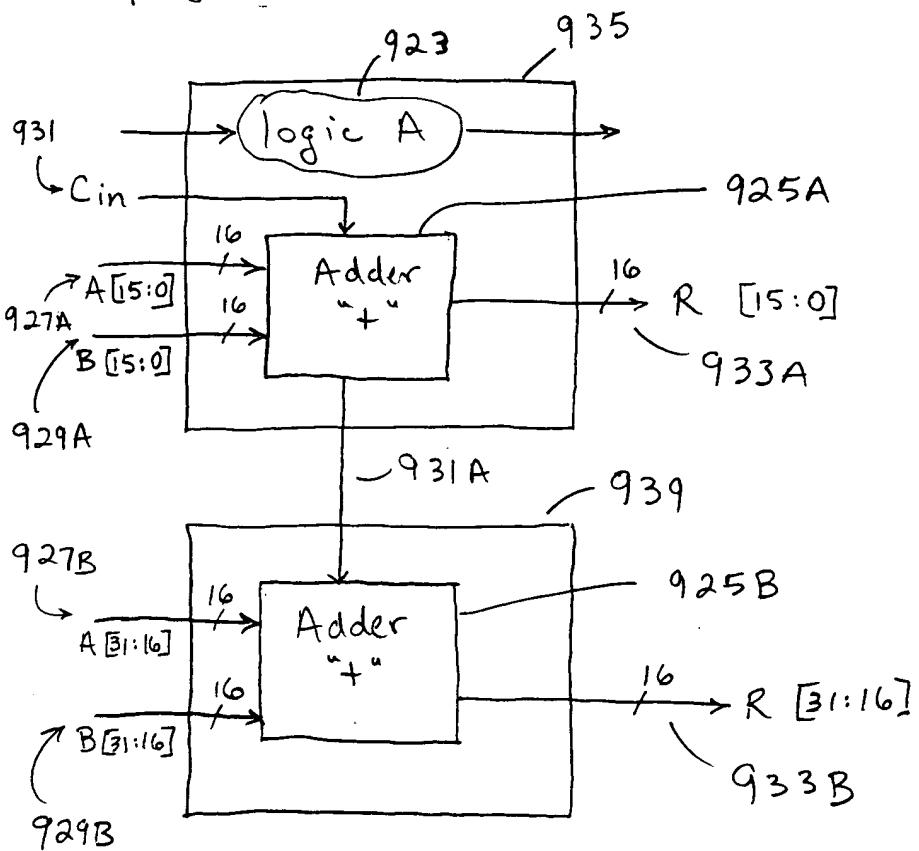


FIG. 10E

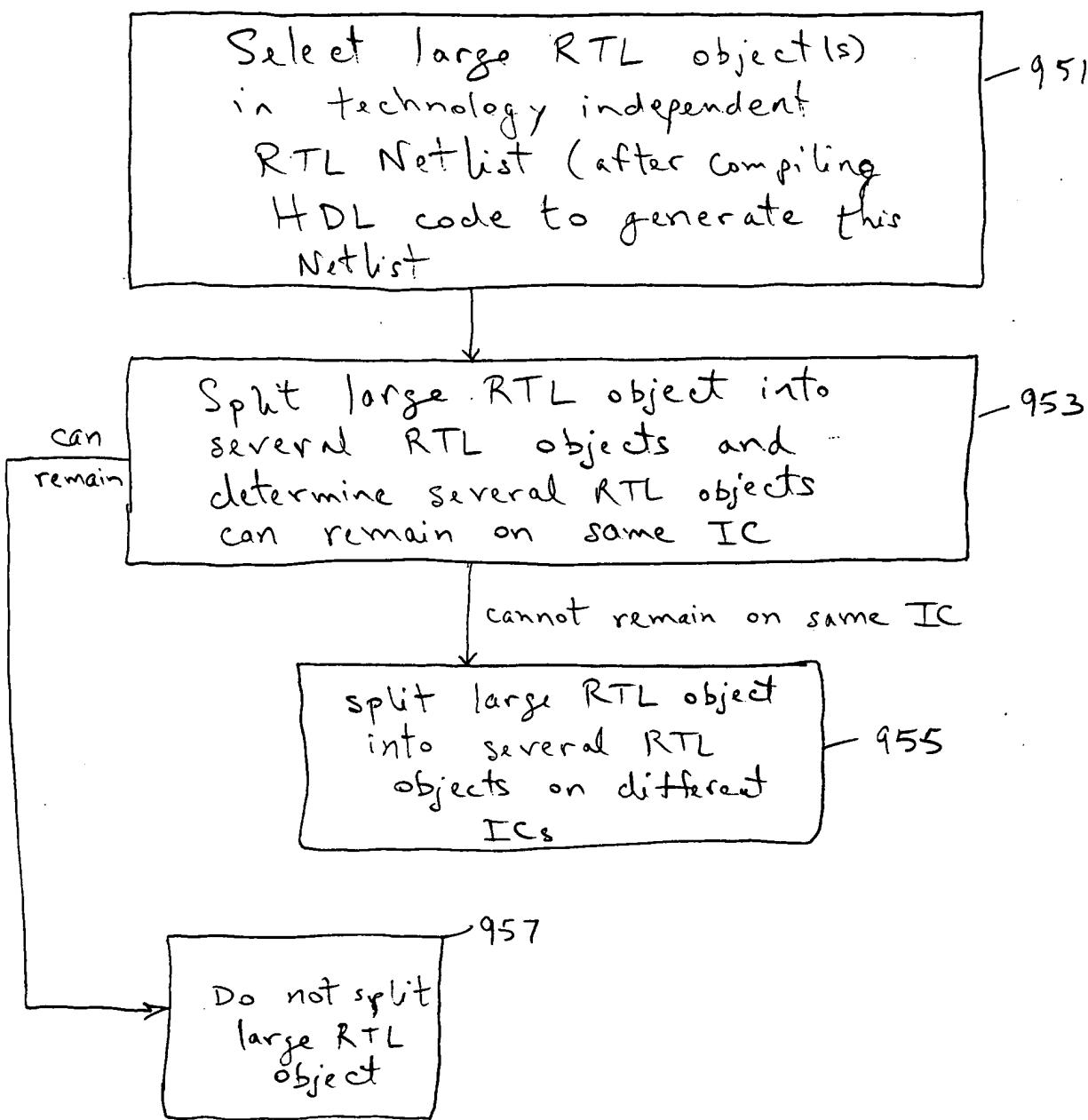


FIG. 11A

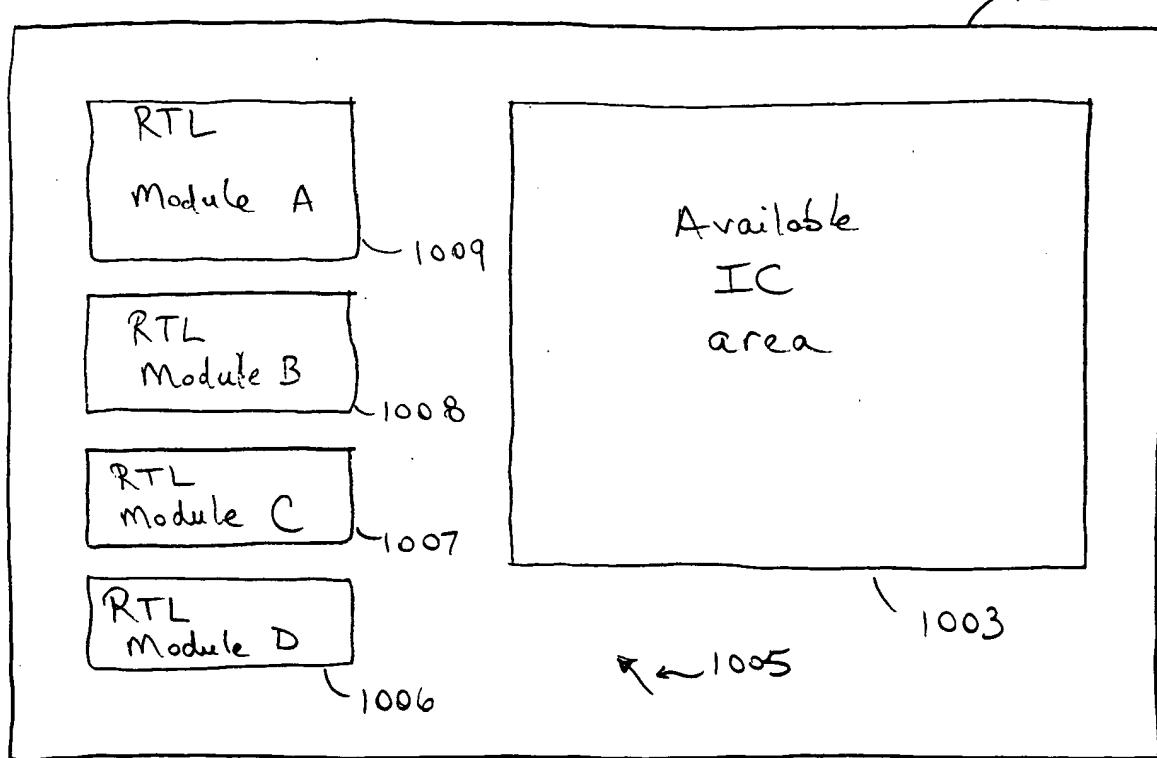


FIG. 11B

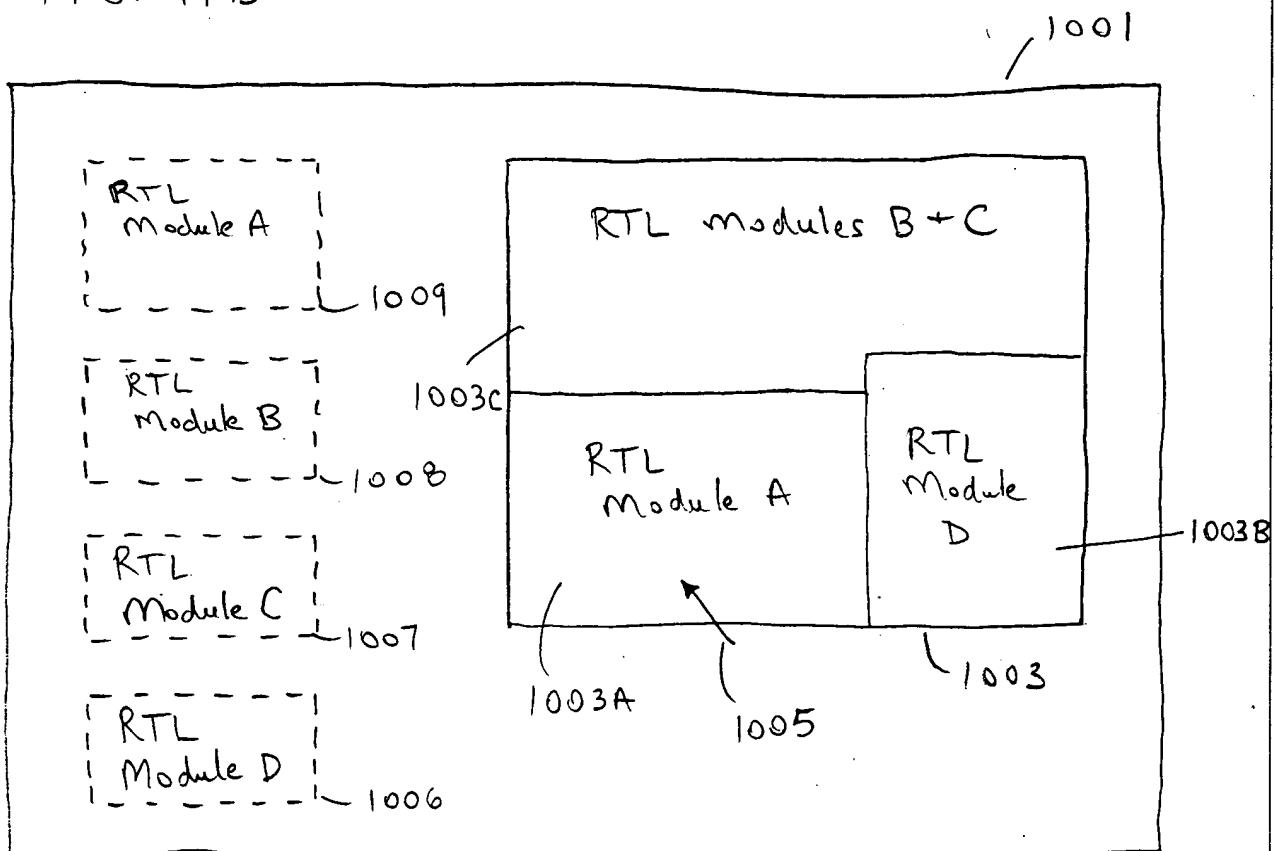


FIG. 12

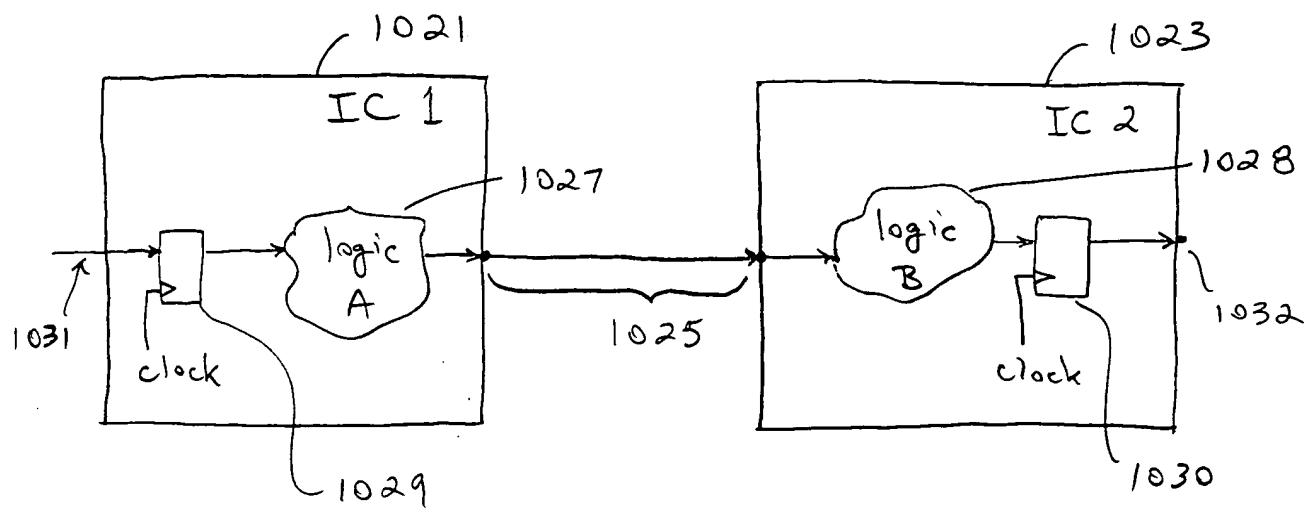


FIG. 13

